IDEC Chip Design Contest

A Framed Pulse Width Modulation(FPWM) Transceiver under Low Supply Voltage Domain

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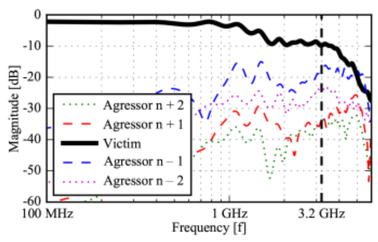
Background

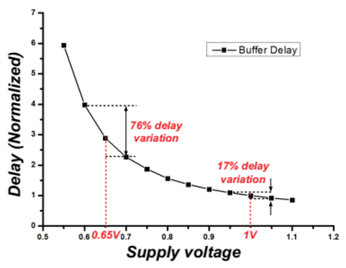
- **Power is Cost**



- **Speed & Power Trade off**



<Channel Loss (DRAM)>

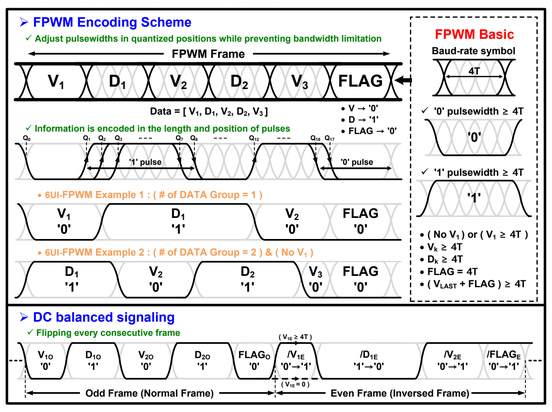


<Bandwidth vs. VDD>

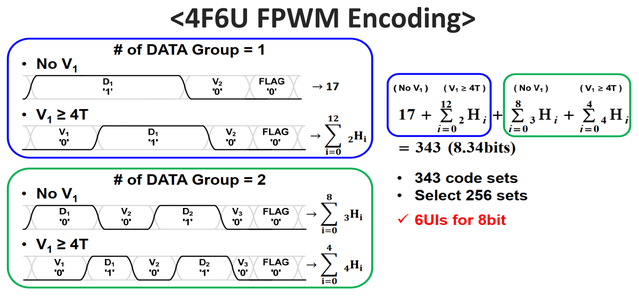
- More speed, more Power
- EQ needs additional Power
- Low VDD limits BW_{IC}

Framed Pulse Width Modulation

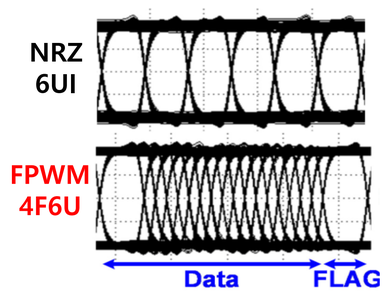
- **Previous work**



<4F6U FPWM Encoding>



<4F6U FPWM Data Sets >



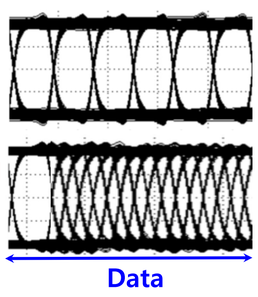
<Eye Diagram of NRZ & FPWM> (4F6U)

$$\text{Coding Gain} = \frac{8\text{bit} - 6UI}{6UI} \times 100\% = 33\%$$

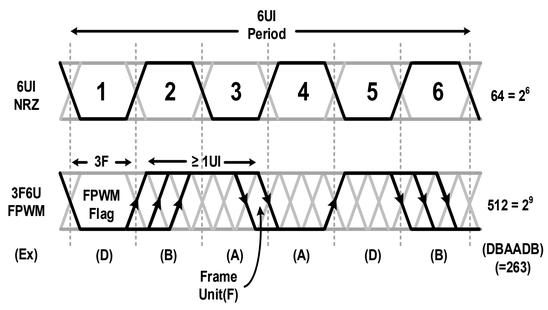
- 33% more bits than NRZ
- LUT based Encoding
- TSMC 40nm CMOS

Revised FPWM and Transceiver IC Architecture

- **Revised Encoding**



<Eye Diagram of NRZ & FPWM> (3F6U)

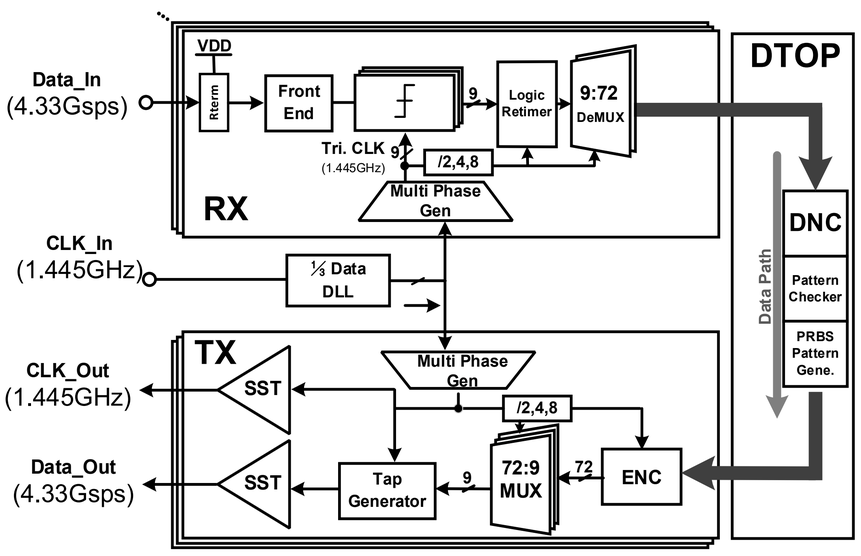


<3F6U FPWM Coding Scheme>

$$\text{Coding Gain} = \frac{9\text{bit} - 6UI}{6UI} \times 100\% = 50\%$$

- 50% more bits than NRZ
- $Data_{pre}$ Succesive Pattern based Encoder
- Samsung 65nm CMOS

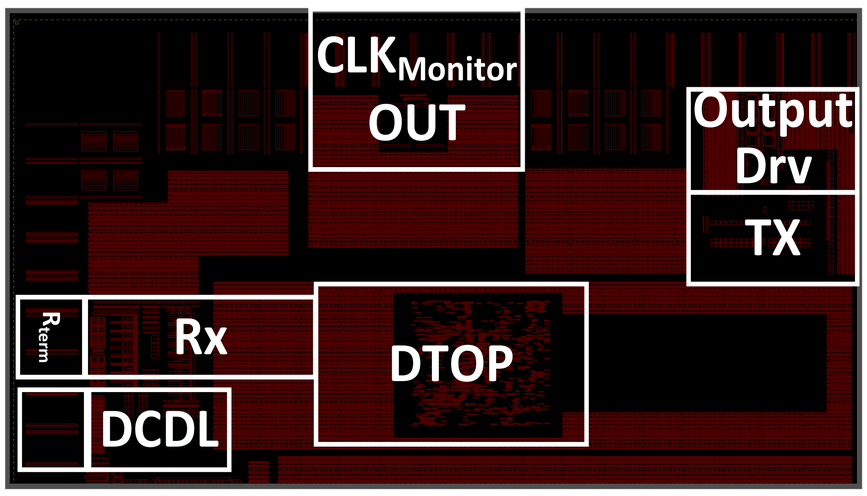
- **Top Architecture**



- **Features**

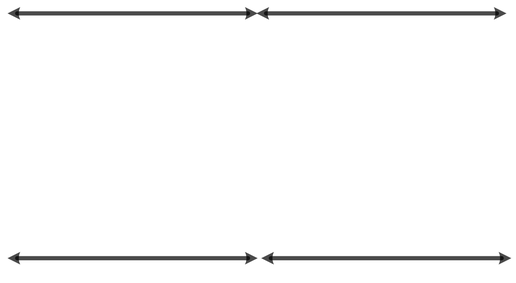
- Spectral Efficiency
  4.33GSps ➔ **6.5Gbps**
- Forwarded CLK & DLL
- PRBS based Encoder /Decoder & Checker
- Samsung 65nm CMOS

IC Layout & Area

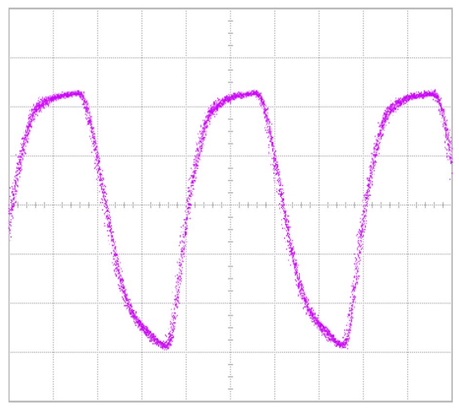


Block	Area(um X um)	Block	Area(um X um)
Rx	460 um X 350 um	CLK	460 um X 96 um
Tx	450 um X 740 um	DTOP	480 um X 510 um

Simulation & Measurement



<Simulated Eye Diagram (4.33Gsps) >



<Forwarded CLK Output >

- Revision Issue : Tx Mux & Output Drv / Rx FE/Samplers
- DLL Loop

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